APPLICATION OF PECVD-SIC AS INTERMEDIATE LAYER IN CRYSTALLINE SILICON THIN-FILM SOLAR CELLS

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ABSTRACT

We present first results on the application of PECVD silicon carbide as intermediate layer for crystalline silicon thin-film solar cells. Silicon carbide layers were deposited by PECVD and characterized by Auger spectrometry and SEM. The subsequent sample processing included high-temperature anneal, deposition of a silicon seeding layer by CVD, recrystallization of the seeding layer by zone-melting, epitaxial growth of the base layer and finally a solar cell process where conventional and one-side contact scheme were realized. All process steps were successfully accomplished but characterization of the samples revealed that the silicon carbide intermediate layers were partly damaged or perforated. Efficiencies up to 7.1 % were reached using a conventional contact scheme.

1. INTRODUCTION

The basic motivation for the development of crystalline silicon thin-film solar cells is the potential to save costs while keeping the efficiency on a level comparable to wafer silicon solar cells. In recent years much effort has been put into research on thin-film structures on various conductive and non-conductive substrates [1], [2]. However the realization of an industrially feasible one-side contact scheme for electrically isolating substrates represents a severe problem [3]. The realization of a thin-film wafer equivalent which can be processed by state-of-the-art techniques is a key issue to bring thin-film solar cells closer to industrial production. Within the high-temperature approach the epitaxial cell on inexpensive silicon substrates and solar cells based on recrystallized silicon layers on foreign conductive substrates can a priori be processed by conventional techniques.

The work presented here is based on the latter concept with focus on the development of an electrical conductive intermediate layer. Silicon carbide represents an attractive option for this application. High purity crystalline silicon carbide is mechanically stable up to high temperatures, it can be made electrical conducting, it is chemically resistant to many alkaline and acid solutions and it is known for its excellent thermo-shock resistivity [4], [5], [6].

2. PECVD OF SILICON CARBIDE

2.1 Deposition by PECVD

The deposition of silicon carbide by plasma-enhanced chemical vapor deposition (PECVD) results in amorphous layers typically containing large amounts of hydrogen. Despite the low deposition temperatures of 300–500°C which are generally used for PECVD many properties of crystalline silicon carbide are preserved [7]. In addition the dependence of the silicon carbide properties on the process conditions allows a tailoring of the layer properties [8].

Typical deposition rates achieved by conventional PECVD are in the range of several nm/min. For industrial production however high throughput is required. Using PECVD this can be achieved by large wafer size capability and high deposition rates, the latter being realized by higher process temperatures [9].

For the deposition of silicon carbide layers we used a parallel plate RF (13.56 MHz) PECVD reactor which is capable to operate at electrode temperatures up to 650°C. The corresponding sample temperature is assumed to range below this value. The powered electrode has a diameter of 250 mm and is located at a distance of 80 mm from the sample electrode. Silane (SiH_4) and methane (CH_4) are used as process gases and nitrogen (N_2) is added for doping. The electrode temperature was kept at 650°C for all depositions.

2.2 Characterization of silicon carbide layers

For characterization two layer types have been grown under different process conditions. In Table I the growth parameters for both process types P1 and P2 are listed.

Table I. PECVD parameters for two deposition processes used for characterization.

process no.	SiH4 [sccm]	CH4 [sccm]	N2 [sccm]	p [mbar]	$T_{electrode}$ [°C]	RF-power [W]
P1	15	91	0.5	0.075	650	250
P2	15	91	0.5	0.065	650	300

Carbon and silicon content and depth profiles were obtained from Auger electron spectroscopy (AES). In Fig. 1 the measured AES profile for sample type P1 and P2 are depicted. The increase in silicon content represents the onset of the underlying silicon substrate.

Calculation of the ratio of silicon to carbon content from both profiles gives a value of 1.94±0.14 and 1.16±0.16 for process P1 and P2 respectively. According to these values the SiC layers grown in process P1 are silicon-rich whereas process P2 results in layers with a nearly stoichiometric composition.

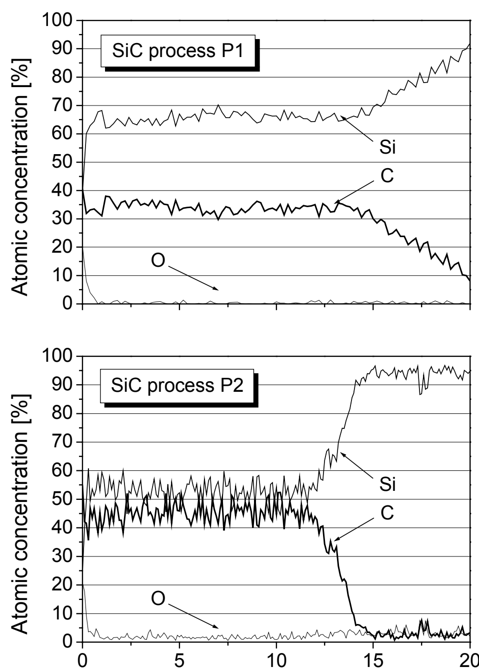

Fig. 1: AES depth profile for silicon carbide layers deposited by process P1 (top) and P2 (bottom).

3. SAMPLE PREPARATION

3.1 Silicon carbide intermediate layer

For solar cell preparation two different processes have been used for the deposition of silicon carbide intermediate layers. The first process is identical to P1 in Table I. For the second process the gas flow rates were increased to 30 sccm SiH_4, 140 sccm CH_4 and 1.2 sccm N_2. The electrode temperature was again fixed to 650°C with an RF-power of 200 W and a pressure of 0.1 mbar. The layer thickness was determined to 120 to 170 nm. In the following both sample types will be referred to sample type A.

For comparison silicon carbide layers deposited at low temperatures were supplied by the Delft Institute of Microelectronics and Submicron Technology (DIMES) (sample type B). These layers are usually used as window layers in p-i-n solar cells. Doping of the layers was achieved by adding diborane to the process gas. The layer thickness ranged between 100 and 500 nm.

After intermediate layer deposition all samples (type A and B) were treated by a high-temperature annealing step at 1250°C under argon atmosphere. This process step was included to enable a possible evaporation of hydrogen and thus to densify the layers [10], [11].

3.2 Seeding layer deposition

Silicon seeding layer deposition was done by APCVD at 950°C. Layers of 10 µm thickness and a doping density of $2x10^{18}$ cm^{-3} were grown at a rate of 1 µm/min. These layers serve as back surface field (BSF) in the final solar cell structure.

For sample type A the surface morphology of the deposited layers was found to be comparable to standard seeding layers grown on SiO_2. SEM analysis on cross sections revealed closed SiC layers with a planar interface between silicon carbide layer and substrate decorated with small cubic-like crystallites (Fig. 2).

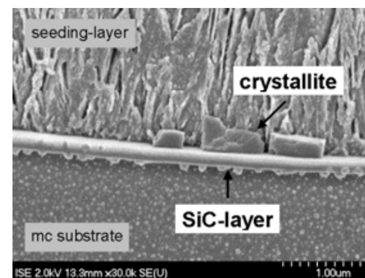

Fig. 2: Cross section SEM image of sample type A. The silicon carbide layer is dense and planar.

For sample type B an increased density of whiskers was observed in the silicon seeding layers. The silicon carbide layers were found to be more or less closed with interface structures from planar to very rough. Cavities below the silicon carbide layer as well as crystallites decorating the interface were observed (Fig. 3).

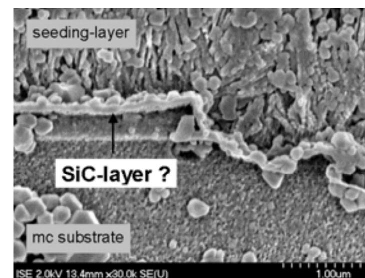

Fig. 3: Sample type B with damaged silicon carbide intermediate layer (SEM image).

3.3 Recrystallization by zone-melting

Prior to ZMR a silicon dioxide capping layer was deposited on top of the seeding layer to prevent balling-up of the molten silicon. In-situ observations of the solidification front morphology during ZMR showed a planar interface. Typical features of the recrystallized silicon layers were grains of several millimeters to centimeters in length and a few millimeters in width. The crystal growth was not ideal but no principle problems were encountered during ZMR.

3.4 Deposition of the base layer

After recrystallization the capping layer was removed by HF and a KOH etch was used for pre-epitaxial surface conditioning and to reveal the grain structure. Epitaxial deposition of the base layer was done at 1170°C with growth rates of 7 µm/min. The dopant gas flow was adjusted to yield a doping level of $5x10^{16}$ cm^{-3} in the base layer.

The status of the silicon carbide layer was inspected by SEM after epitaxy. The SEM image in Fig. 4 shows sample type A with a porous silicon carbide layer and a crack penetrating the recrystallized seeding layer. A typical outstanding feature for samples of Type B is the presence of large cavities underneath the silicon layer system and crystallites which fill the cavity in some

places. In general the morphology of the intermediate silicon carbide layer ranged from a dense to porous or even damaged structure. Again a decoration with crystallites can be observed.

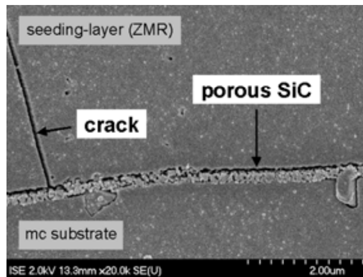

Fig. 4: SEM image of a sample cross section (type A) after recrystallization and epitaxy. The silicon carbide layer is now porous and a crack penetrates the seeding layer.

Spreading resistance measurements were carried out for a characterization of the doping-profiles across the entire layer system. In Fig. 5 doping profiles measured on three different samples are shown.

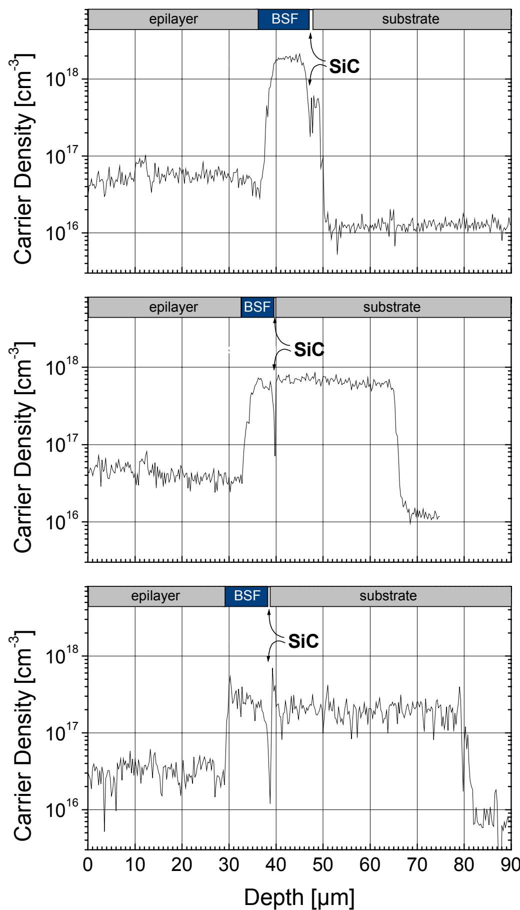

Fig. 5: SRP doping profiles measured on recrystallized and epitaxied samples. Perforation of the intermediate SiC layer results in a diffusion of boron atoms from the seeding layer (BSF) into the molten part of the substrate. The highly doped substrate region below the SiC corresponds to the penetration depth of the molten zone.

The top and bottom profile correspond to sample type A whereas the profile in the middle was measured on sample type B. These are local measurements and do not necessarily represent the properties of the entire sample.

The location of the silicon carbide intermediate layer can be identified by a sharp drop in carrier density between back surface field (BSF) and substrate. The specific resistance of the silicon substrates was specified to 1 Ωcm. However the doping level of the substrate region below the silicon carbide layer is much greater than this value in fact it is identical to the doping level of the recrystallized seeding layer. The sequence of doping profiles illustrated in Fig. 5 demonstrates that a deeper penetration of the highly doped region into the substrate is combined with a lower doping-level. This effect can be explained by the observed porosity or even perforation of the silicon carbide layers. During ZMR boron atoms can diffuse from the liquid seeding layer into the molten part of the substrate. The depth of the highly doped region reaching into the substrate surface layer therefore indicates the penetration of the melting zone into the substrate material. Comparing the SRP profiles it cannot be concluded that a deeper penetration depth corresponds to a larger porosity of the silicon carbide layer. In fact no explicit conclusions can be drawn on a possible difference in properties for the different types of silicon carbide layers.

4. SOLAR CELLS

4.1 Solar cell contact scheme

Conventional and one-side contact solar cell structures were realized on each sample simultaneously. For electrical conductive silicon carbide layers a conventional contacting of the cell should be possible. The resistivity of the intermediate layers could not be determined before solar cell processing therefore the one-side contact scheme was additionally realized. In Fig. 6 the solar cell structure is illustrated.

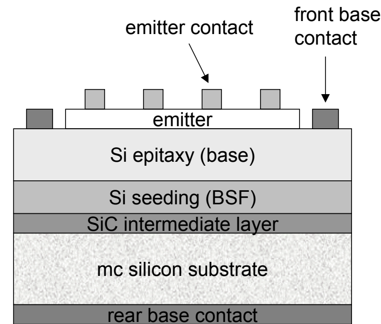

Fig. 6: Solar cell with front-front and rear-front contact schemes realized.

4.2 Solar cell results

The solar cell process included a random texturing of the surface by KOH etching, remote plasma hydrogen passivation and a double layer antireflection coating. FZ-Si material (0.5 Ωcm) was used for reference cells. In

Table II the best results achieved for solar cells with silicon carbide intermediate layers are listed. For comparison the solar cell parameters for both contact types are given.

Table II: Parameters of the best solar cell with silicon carbide intermediate layer.

		V_{oc} [mV]	I_{sc} [mA/cm²]	FF [%]	η [%]
front-front	SiC-IL	488	21.7	65.1	6.9
	*Ref.**	*635*	*33.2*	*79.6*	*16.8*
front-back	SiC-IL	488	22.3	65.1	7.1
	*Ref.**	*634*	*34.1*	*78.8*	*17.0*

Solar cell area: 1 cm²

** References: FZ-silicon, 0.5 Ωcm*

Independent on the silicon carbide sample type the solar cell parameters for both contact schemes differ only slightly in terms of short-circuit current and fill factor. This result does not prove the electrical conductivity of the silicon carbide intermediate layers it rather confirms the porosity or perforation already observed by SEM and especially SRP.

An analysis of the fitted dark I-V parameters of the solar cells showed that low open-circuit voltage and fill factors can be traced back to increased values for I_{02}. In addition comparatively low short-circuit currents were measured for all cells. These observations can be attributed to the low crystal quality of the recrystallized layers resulting from a non-ideal crystal growth during ZMR.

5. CONCLUSION

Silicon carbide layers were deposited by PECVD and used as intermediate layers for crystalline silicon thin-film solar cells. Silicon seeding layer deposition, zone-melting recrystallization and epitaxial growth of the base layer were successfully accomplished on these substrates. Characterization of the samples showed that the silicon carbide layers were not completely stable to the entire process sequence. First solar cells were manufactured leading to a maximum efficiency of 7.1% using a conventional contact scheme.

To the authors knowledge these are the very first thin-film solar cells where a PECVD silicon carbide film is applied as intermediate layer. The results gained in this work show that these layers can in principle be used in silicon thin-film solar cell processing. Future activities will focus on the optimization of the silicon carbide layer properties in terms of stability to the herein presented process sequence and in terms of electrical conductivity.

6. ACKNOWLEDGEMENTS

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