

SILICON FILMS ON CERAMIC SUBSTRATES (SOCS): GROWTH AND SOLAR CELLS

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ABSTRACT

In this work, we review the different steps of formation of silicon thin film solar cells on different ceramics, namely mullite, SiSiC and SiN. The p+ silicon seeding layer is obtained by high-temperature CVD followed by zone-melting recrystallization (ZMR) in order to enlarge the grains. The active p doped silicon layer is formed by epitaxy on the recrystallized Si film. The structural and electrical properties of the different layers are presented and the diffusion of contaminants from the ceramic substrates into the silicon film was investigated. Solar cells were prepared on such SOCS structures and their photovoltaic properties were evaluated.

1. INTRODUCTION

Crystalline silicon thin films on ceramic substrates (SOCS) can be considered as a very promising alternative to bulk silicon based cells [1]. Cost reductions can be accomplished in the processing and the amount of silicon used. On the other hand, following the high-temperature approach a large number of requirements are imposed on the substrate (properties). It should provide a thermal expansion coefficient similar to that of silicon (approximately $4 \times 10^{-6} \text{ K}^{-1}$) to avoid any peeling off the as-grown silicon layer. In addition the substrate has to be chemical inert towards process gases used for CVD and towards liquid silicon and it has to be mechanically stable up to the melting point of Si. It should inhibit any out-diffusion of substrate impurities into the active silicon layer during the deposition process to avoid formation of electrically active recombination centers in this layer. Additional barrier layers would then be necessary to prevent diffusion. Another important criterion for PV is low manufacturing cost and large area fabrication. So far, no commercial materials are able to fulfil all these requirements. The option is limited to a couple of substrates such as high temperature glass [2], graphite [3], aluminum based ceramics like alumina (Al_2O_3) [4], SiAlON [5], mullite ($3\text{Al}_2\text{O}_3 \cdot 2\text{SiO}_2$) [6,7] and silicon based ceramics such as Si infiltrated silicon carbide (SiSiC) [8] and silicon nitride (SiN) [9]. Most ceramics can be produced in large sheets from slurry by the tape cast-method or the doctor-blade process [10]. Sheets of 1.5 m width are possible. This technique has the potential of further reducing the costs of ceramic substrates, and therefore of Si thin-film based solar cells (SOCS).

In this paper we report on the application of ceramic SiSiC, SiN and mullite substrates for silicon thin-film solar cells.

2. PREPARATION OF SOCS STRUCTURES

2.1. Ceramic substrates

Table 1 gives the main properties of the ceramic substrates used in this study and compares them to those of silicon. The SiSiC, SiN and mullite substrates were provided by H.C. Starck ceramics, (Germany) and CIM (Spain), respectively. These substrates offer the advantages to be thermally stable and to sustain high temperatures up to the melting point of silicon. More important they have a thermal expansion coefficient very close to that of silicon.

Comparing the substrate properties mullite differs from the remaining materials by its high reflectivity in the long-wavelength region, which is crucial for an effective optical confinement [11].

Table 1 Main properties of potential ceramic substrates and compared to those of silicon.

Parameters	Si	SiSiC	SiN	Mullite
Density (gcm^{-3})	2.32	3.1	3.22	3.16
Open porosity (%)	-	<1	<1	<3
Therm. Exp. 20-1000°C (10^{-6} K^{-1})	3.9	4.0	3.4	5
Therm. Cond. 20°C (W/mK)	140	110	22	7
Specific heat (J/KgK)	700	900	700	500
Max. Temp. (°C)	1410	1400	1750	1700
Reflectivity at 900nm (%)	35	17	55	85

2.2. Impurity diffusion and barrier layers

When silicon deposition at high temperature and zone-melting recrystallization are performed on a foreign substrate, one important concern is the possible contamination of the silicon layer by solid diffusion of impurities (mainly metals) from the substrate [12]. We have probed the diffusion of contaminants from the ceramic substrates into silicon by SIMS and DLTS (Deep Level Transient Spectroscopy). P-type Cz-Si samples were brought into contact with each ceramic substrate and heated up to 1200°C for 3 min under nitrogen (typical deposition conditions). For DLTS, a Schottky diode was used as a probe. The DLTS is a very sensitive method to study deep levels in semiconductors. The method is based on the capacitance change of a reverse biased diode when

deep levels emit their carriers after they were charged by a forward bias pulse. The emission rate is temperature dependent and characteristic for each type of defect. From the temperature dependence of the emission rate the activation energy of a deep level can be deduced.

Figure 1 compares DLTS spectra obtained on silicon samples contaminated by SiSiC, SiN and mullite substrates. Many traps can be detected. Plotting the emission rates versus temperature of the peaks led to the characteristics of the traps. Although DLTS is unable to give the chemical signature of the detected point defects, activation energies and cross sections of the observed traps allow us to speculate that the main contaminants are transition metals: Mn, Co, Cr and more likely Fe [13]. The substrate SiSiC is found to be more contaminated than the SiN and mullite. For instance, iron density in the range $4\text{-}5 \times 10^{14} \text{ cm}^{-2}$ was detected in Si contaminated by SiSiC compared to $0.8\text{-}1 \times 10^{14} \text{ cm}^{-2}$ and $3\text{-}5 \times 10^{13} \text{ cm}^{-2}$ in Si contaminated by SiN and mullite, respectively. SIMS analysis revealed a high amount of boron concentration present in SiSiC compared to SiN and mullite, thus making the SiSiC ceramic even conductive.

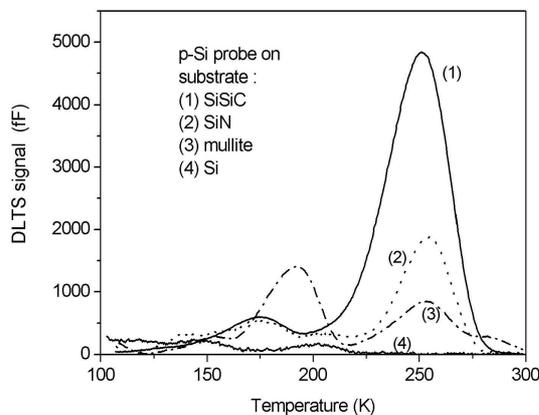


Fig. 1 DLTS spectra as measured on Schottky diodes prepared on Si probes, which were in contact to different ceramic substrates and heated at 1200°C for 3min when on top of different ceramic substrates. The emission rate is 200/s.

In order to avoid out-diffusion of the metals during silicon deposition and further processes, the ceramics have to be coated with an efficient diffusion barrier layer. In this work, we used two different barriers on the ceramics: (i) three consecutive layers composed of $2\mu\text{m}$ oxide- $0.2\mu\text{m}$ nitride and $2\mu\text{m}$ oxide (ONO) which have been deposited by PECVD at 350°C ; (ii) a single silicate glass film obtained by spinning a SOG solution (Filmtronics 700A). The efficiency of such barrier layers has been tested using the same experiment as above, but replacing the bare ceramics by coated ones [13]. For both barrier layers, the DLTS spectra show a strong reduction in the peak heights which reach the level of the reference silicon sample (Figure 2). These results indicate that such barrier layers are sufficient to stop diffusion of impurities towards the silicon layer during deposition and subsequent melting.

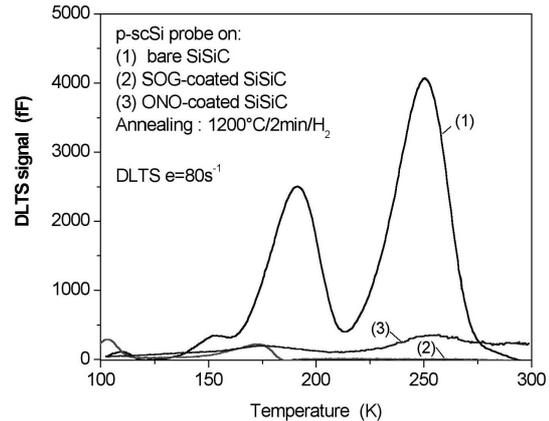


Fig. 2 DLTS spectra of p-type silicon probe samples after annealing at 1200°C for 3min on bare, ONO and SOG coated SiSiC substrate. The emission rate is 80 s^{-1} .

2.3. Silicon seeding and active layers

The structure of the crystalline silicon thin film solar cell on ceramics is n^+pp^+ . First, the p^+ -Si layer, $6\text{-}8\mu\text{m}$ thick, was deposited on ONO or SOG coated ceramics at 1050°C in an Atmospheric Pressure Chemical Vapor Deposition (APCVD) reactor which uses trichlorosilane as silicon precursor and trichloroborane as doping source. This highly doped silicon layer serves as a seeding layer for subsequent recrystallization and also builds up a back surface field thus reducing the rear surface recombination. The high temperature deposition results in fine-grained silicon with average size of $3\text{-}5\mu\text{m}$ and a boron doping level of $\sim 5 \times 10^{20} \text{ at.cm}^{-3}$ and $\sim 5 \times 10^{18} \text{ at.cm}^{-3}$, for SiSiC and SiN respectively. We believe that the much higher boron concentration in the p^+ -Si layer is caused by the out-diffusion of boron from SiSiC during silicon deposition at high temperature.

After seeding layer deposition zone-melting recrystallization step was applied to enlarge the grains [14]. Prior to ZMR $2\mu\text{m}$ of SiO_2 were deposited onto the p^+ silicon seeding layer to prevent balling-up of the liquid silicon. Then the layer was recrystallized at a speed of $\sim 10 \text{ mm/min}$ in an Ar/O_2 atmosphere using focused halogen lamps. The resulting grains are about 1-3 mm wide and 1-3 cm long.

The active p-Si layer was formed by epitaxy using an atmospheric pressure chemical vapour deposition reactor which offers the possibility of deposition rates up to $5 \mu\text{m/min}$. Typical epilayer thickness is $\sim 10\text{-}12 \mu\text{m}$. The doping level in the p-layer was controlled by varying the BCl_3 flow in the reactor during epitaxy.

Figures 3a and 3b exhibit optical microscope cross-section images of a $15\text{-}18 \mu\text{m}$ thick silicon layer formed on SiSiC and SiN substrates, respectively. A Secco etch of 36 sec has been used in order to reveal the dislocations and to distinguish between the differently doped silicon layers. Thus, the ONO layer as well as the p^+ and p layers is well identified in Figure 3. It is clear that the Si adheres perfectly on the coated substrates despite surface irregularities and even open pores onto the starting ceramic surface. Similar images are obtained for silicon on coated mullite (Filmtronics) ceramics. The intermediate ONO layer was not perturbed after the recrystallization procedure. However, some cracks in the Si layer were observed when SiN substrates were used,

probably because of the lower thermal expansion coefficient compared to silicon (Table 1). Besides, some discontinuities in the ONO layer were observed which might induce impurities into the silicon layer system.

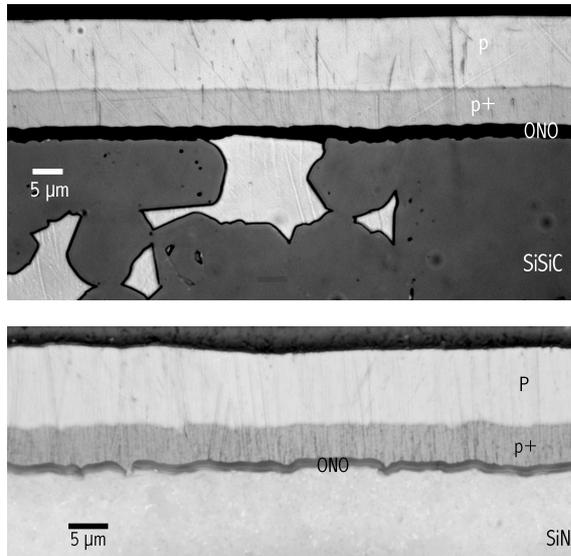


Fig. 3 A cross-section optical image of a 6 μm $\text{p}^+\text{-Si}$ / 12 μm p-Si structure deposited onto 2 μm thick coated ONO (a) SiSiC and (b) SiN substrates.

Figure 4 shows the carrier concentration profiles as measured by the spreading resistance technique on the $\text{pSi-p}^+\text{Si}$ -ceramic structures. The flow of the doping gas (BCl_3) was fixed to 80 sccm and 5 sccm during the seeding layer deposition and epitaxy, respectively. This corresponds to a doping level of about 10^{17} cm^{-3} in the epilayer, and about $5\text{-}8 \times 10^{18} \text{ cm}^{-3}$ in the seeding layer. A high/low doping transition is therefore formed, creating a back surface field at the interface. In the case of SiSiC substrate, the strong difference between the carrier concentration determined by SRP and the total boron concentration deduced from SIMS indicates that a large amount of boron atoms in the p^+ layer is not electrically active.

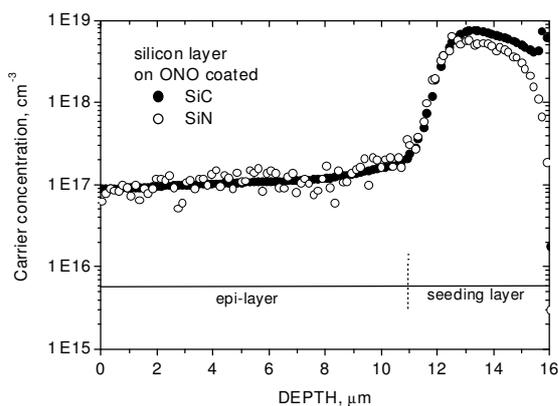


Fig. 4. Carrier concentration profile obtained by spreading resistance measurements of p-p^+ structures as made on SiSiC and SiN ceramic substrates.

3. SOCS BASED SOLAR CELLS

For solar cell preparation the n-type emitter region was realized by rapid thermal diffusion from phosphorus

doped spin-on glass source. The thermal processing was carried out at 900 $^\circ\text{C}$ for 90 sec resulting in a sheet resistance of about 40 Ohms per square. No additional gettering was performed.

Due to the insulating barrier layers, emitter and base were contacted on the front side. Figure 5 gives a schematic view of the test SOCS based solar cells. Access to the base was possible by plasma etching around the cell, thus forming a $1 \times 1 \text{ cm}^2$ mesa cell. Metallization was done by aluminum evaporation through a grid mask for front contact and for back contact. Finally, an 80 nm SiN:H layer was deposited by remote plasma deposition on the cell to serve as a passivation and an antireflection coating layer.

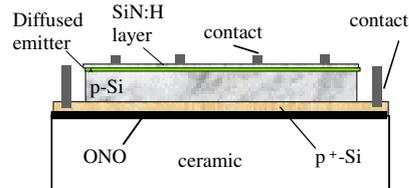


Fig. 5 A schematic view of the SOCS based solar cells.

Figure 6 plots the external quantum efficiency (EQE) of silicon on SiN solar cells for different flow of the doping gas BCl_3 during epitaxy. From SIMS and SRP measurements, the flow values of 5, 15 and 25 sccm correspond to 10^{17} , 5×10^{17} and $2 \times 10^{18} \text{ Boron/cm}^3$, respectively. As the doping level in the active layer increases, the bulk minority carrier diffusion length strongly decreases, resulting in a dramatic reduction in spectral response. Even for moderate doping, the measured cells show bad spectral response in the short-wavelength region as well as in the long-wavelength region. The low response in the blue can be attributed to a non-optimized emitter as well as to a high surface recombination velocity. The low effective minority carrier diffusion length being responsible for the poor long-wavelength response is probably caused by micro-cracks in the Si layer and/or by contamination.

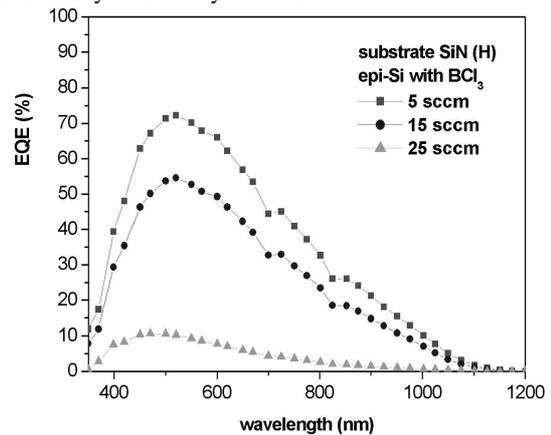


Fig. 6. Spectral response of silicon solar cells on SiN ceramic prepared with different doping level in the epilayer.

Figure 7 compares the internal quantum efficiency (IQE) of 15 μm thick silicon solar cells prepared on different ceramic substrates. Solar cells on mullite show the best spectral response. A large benefit of the high reflectance

from the mullite substrate is clearly visible on the IQE in the near infrared region. In contrast, the IQE data of cells on SiN and SiSiC are quite low. The estimated minority carriers diffusion lengths are about 10 and 15 μm , for SiSiC and SiN respectively. Improvement in the Si layer quality is therefore still necessary. Cells on SiN substrates suffer from cracks in the Si layer whereas the quality of the cell on SiSiC is limited by the high density of defects in the active layer. More importantly, the lack of optical confinement, from front and back side, is detrimental to the SiN and SiSiC based cells. Thus, the optical confinement is of high importance for such structures [9].

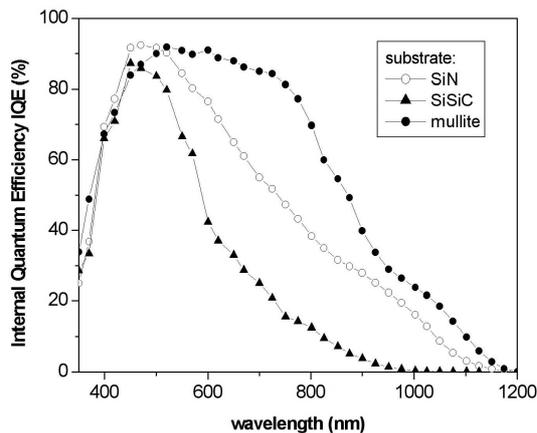


Fig. 7 Internal quantum efficiency of thin film silicon solar cells prepared on different ceramic substrates.

4. SUMMARY

Crystalline silicon thin films (SOCS) have been prepared on SiN, SiSiC and mullite ceramic substrates. Such ceramics offer the advantages of mechanical hardness, chemical and thermal stability during silicon deposition and zone-melting recrystallization. Barrier layers like ONO and SOG have been shown to stop out-diffusion of metals from the substrates. Large-grained silicon layers were achieved by deposition of a seeding layer and subsequent zone-melting recrystallization, followed by a high temperature epitaxy. Test solar cells with a base layer thickness of 20 μm were prepared on such SOCS structures resulting in a poor spectral response for SiN and SiSiC. For mullite, the spectral response was significantly improved thanks to an efficient optical confinement from the back. Present activities focus on an improvement in silicon film quality. Ceramic substrates seem to be a very promising approach for crystalline silicon thin film solar cell manufacturing.

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